a divider, wherein the VCO comprises a pair of cross-coupled transistors, an inductor coupled to the cross-coupled transistors, and a filtering circuit having a capacitor and a variable resistor.

2. (Original) The high-speed bit stream data conversion circuit of Claim 1, wherein the filtering circuit reduces noise contained within a bias voltage provided to the VCO.

3. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the filtering circuit reduces 1/f noise and white noise.

4. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the resistor within the filtering circuit acts to reduce the voltage applied to the VCO core.

5. (Original) The high-speed bit stream data conversion circuit of Claim 1, wherein the VCO circuit further comprises a second resistor to adjust VCTR voltage.

6. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the plurality of inputs further comprise:

a Loop Timing Clock Signal;

an External Reference Clock Signal; or

a Reverse Clock Signal provided by an external data conversion circuit.

7. (Withdrawn) The high speed bit stream data conversion circuit of Claim 1, wherein the first data conversion data conversion circuit multiplexes the at least one first bit stream into the at least one second bit stream.

8. (Withdrawn) The high speed bit stream data conversion circuit of Claim 7, further comprising a second data conversion data conversion circuit that receives the at least one second bit stream at the second bit rate and multiplexes into at least one third bit streams at a third bit rate, wherein the number of the at least one third bit streams is less than the number of the at

least one second bit streams, and the bit rate of the at least one third bit stream and exceeds the bit rate of the at least one second bit stream.

9. (Withdrawn) The high speed bit stream data conversion circuit of Claim 8, wherein a selectable forward/reverse clock relationship exists between the first data conversion data conversion circuit and the second data conversion circuit.

10. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the clock circuit further comprises a phase detector operable to generate a phase adjustment signal to the first data conversion circuit.

11. (Original) The high speed bit stream data conversion circuit of Claim 1, wherein the first data conversion circuit demultiplexes the at least one first bit stream into the at least one second bit stream.

12. (Original) The high speed bit stream data conversion circuit of Claim 11, further comprising a second data conversion circuit that receives the at least one second bit stream at the second bit rate and demultiplexes the at least one second bit stream into a plurality of third bit streams at a third bit rate, wherein the number of the plurality of third bit streams exceed the number of the at least one second bit streams, and the bit rate of the at least one second bit stream and exceeds the bit rate of the plurality of third bit streams.

13. (Original) The high speed bit stream data conversion circuit of Claim 12, wherein a switchable master/slave relationship exists between the first data conversion circuit and the second data conversion circuit.

14. (Original) The high speed bit stream data conversion circuit of Claim 13, wherein the clock circuit further comprises a phase detector operable to generate a phase adjustment signal to the first data conversion circuit.

15. (Original) A clock circuit that produces a Reference Clock Signal used to latch data between at least one first bit stream and at least one second bit stream, wherein the number and bit rate of the at least one first bit stream and the at least one second bit stream differ, and wherein the clock circuit comprises:

a phase locked loop (PLL) having a phase detector that receives a plurality of inputs that include the first bit stream data clock and a loop output, wherein the PLL further comprises a charge pump, a loop filter, a Voltage Controlled Oscillator (VCO), and a divider, wherein the VCO comprises a pair of cross-coupled transistors, an inductor coupled to the cross-coupled transistors, a filtering circuit having a capacitor and a first resistor, and a voltage-adjusting resistor.

16. (Original) The clock circuit of Claim 15, wherein the plurality of inputs further comprise:

a Loop Timing Clock Signal;

an External Reference Clock Signal; or

a Reverse Clock Signal provided by an external data conversion circuit.

17. (Original) The clock circuit of Claim 15, wherein the filtering circuit reduces noise contained within a bias voltage provided to the VCO.

18. (Original) The clock circuit of Claim 15, wherein the filtering circuit reduces 1/f noise and white noise.

19. (Original) The clock circuit of Claim 15, wherein the resistors reduces voltage applied to the VCO core.

20. (Original) The clock circuit of Claim 15, wherein the VCO circuit further comprises a second resistor to adjust VCTR voltage.

21. (Original) A method of producing a Reference Clock Signal, within a clock circuit, wherein the Reference Clock Signal is used to latch data between at least one first bit stream and at least one second bit stream, wherein the number and bit rate of the at least one first bit stream and the at least one second bit stream differ, comprising the steps of:

generating with a Voltage Controlled Oscillator (VCO) one of a plurality of inputs to a Phase Locked Loop (PLL) within the clock circuit, wherein the plurality of inputs to the PLL include a first bit stream data clock, and wherein the input provided by the VCO comprises a VCO Output Signal;

reducing noise contained within the VCO Output Signal with a filtering circuit coupled to the VCO, wherein the filtering circuit has a capacitor and a resistor;

selecting from the plurality of inputs to the PLL, an input from which the Reference Clock Signal will be generated; and

generating within the clock circuit, the Reference Clock Signal from the selected input.

22. (Original) The method of Claim 21, further comprising the steps of providing a Loop Timing Clock Signal, an External Reference Clock Signal, and/or a Reverse Clock Signal as the plurality of inputs to the PLL.

23. (Original) The method of Claim 21, wherein the noise contained within the VCO Output Signal is within a bias voltage provided to the VCO.

24. (Original) The method of Claim 21, wherein the step of reducing 1/f noise and white noise from a bias current reduces noise contained within the VCO Output Signal.

25. (Original) The method of Claim 21, further comprising the step of reducing the voltage applied to the VCO core with the resistor of the filtering circuit and a voltage adjusting resistor.

26. (Withdrawn) The method of Claim 24, wherein the Reference Clock Signal is generated within a multistage data conversion circuit used to multiplex at least one first bit streams to at least one second bit stream.

27. (Original) The method of Claim 24, wherein the Reference Clock Signal is generated within a multistage data conversion circuit used to demultiplex at least one first bit streams to at least one second bit stream.